

REMARKS

Status of the Application

Claims 1-20 are pending and stand rejected. Claims 1, 8 and 15 have been amended to more particularly point out the claimed invention and find support in the as-filed application at least at, for example, p. 16, ll. 12-18. No new matter has been added by these amendments.

In view of the foregoing amendments and following remarks, Applicants respectfully request entry of this Amendment Response, reconsideration of the present application and a Notice of Allowance.

Claim Rejection – 35 U.S.C. § 103(a)

Claims 1, 2, 4-6, 8, 9, 12-17, 19 and 20 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schneider, *et al.* (U.S. Pat. No. 5,777,621 and “Schneider” hereinafter) in view of Baldwin (U.S. Pat. No. 5,798,770 and “Baldwin” hereinafter). It is respectfully submitted that claims 1, 2, 4-6, 8, 9, 12-17, 19 and 20 are patentable for the reasons set forth below.

Claims 1, 2, 4-6, 8, 9, 12-17, 19 and 20 include features that are neither disclosed nor suggested by the cited references, taken alone or in combination, namely, as represented by claim 1:

A method for representing a scene, comprising:
providing a higher-level appearance description of an appearance geometry in a retained-mode representation, wherein the higher-level appearance description is created using a first appearance description;
selecting a representational level for a parameter or object in the higher-level appearance description;
defining a temporary storage requirement for a statically-allocated memory resource; and
traversing the retained-mode representation according to the selected representational level *and the defined temporary storage requirement* to provide a final representation that can be rendered by a graphics pipeline.
(Emphasis added).

The present invention as claimed in claim 1 provides a method for representing a scene in a graphics environment. A higher-level appearance description of an appearance

geometry in a retained-mode representation is provided. A representational level for a parameter or object in the higher-level appearance description is selected, and a temporary storage requirement for a statically-allocated memory resource is defined. The retained-mode representation is traversed according to the selected representational level and the defined temporary storage requirement to provide a final representation that can be rendered by a graphics pipeline.

Schneider teaches a graphics rendering system that includes a continuum of quality control data groups, each of which contains a plurality of quality control type variables. Each of the type variables contains a value that selects among a plurality of options in a respective trade-off between rendering quality and rendering speed. Each of the quality control data groups may be associated with the respective quality index, which allows an application to select a point on the overall rendering speed/quality trade-off by selecting a quality control index value.

Baldwin teaches a pipelined graphics processor that dynamically reconfigures a rendering sequence. Pixel elimination sequences such as depth and stencil tests are performed before texturing calculations are performed, so as to remove unneeded pixel data prior to performing texturing calculations.

In contrast to the claimed invention, neither Schneider nor Baldwin, alone or in combination, teach “*defining a temporary storage requirement for a statically-allocated memory resource*” or “traversing [a] retained-mode representation according to [a] selected representational level *and the defined temporary storage requirement* to provide a final representation that can be rendered by a graphics pipeline” as claimed.

As part of the rendering process taught by Schneider, memory space is allocated to contain pointers to “to a set of methods appropriate for all objects in a ‘shared object’ class.” (Col. 11, ll. 5-7). If there are no methods in a particular class, no space is allocated. (See col. 11, ll. 7-9). Enough memory space is allocated for “the private data structures needed for its own Private data plus the Private data for all descendant classes.” (Col. 23, ll. 32-36). As can be seen from the above passages, Schneider allocates memory space *dynamically*, i.e., by only allocating the memory space necessary for a set of methods, and by not allocating memory space when none is needed. At no point does Schneider appear to teach “*defining a temporary storage requirement for a statically-allocated memory resource*,” and

consequently also does not teach “traversing [a] retained-mode representation according to [a] selected representational level *and the defined temporary storage requirement* to provide a final representation that can be rendered by a graphics pipeline” as claimed.

Applicants respectfully submit that Baldwin fails to cure the deficiencies of Schneider. As noted above, Baldwin teaches a pipelined graphics processor for dynamically reconfiguring a rendering sequence. At no point does Baldwin appear to teach “*defining a temporary storage requirement for a statically-allocated memory resource*,” and consequently also does not teach “traversing [a] retained-mode representation according to [a] selected representational level *and the defined temporary storage requirement* to provide a final representation that can be rendered by a graphics pipeline” as claimed. As neither Schneider nor Baldwin individually teach all of the features of amended claim 1, the combination of Schneider and Baldwin also fails to teach all of the features of amended claim 1.

As independent claims 8 and 15 contain features similar to those recited in claim 1, Applicants respectfully submit that Schneider and Baldwin, taken alone or in combination, fail to teach *all* of the limitations of claims 1, 8 and 15. Accordingly, Applicants respectfully submit that claims 1, 8 and 15 patentably define over the cited art. As claims 2 and 4-6 depend from claim 1, claims 9 and 12-14 depend from claim 8 and claims 16, 17 and 19 depend from claim 15, Applicants respectfully submit that claims 2, 4-6, 9, 12-14, 16, 17 and 19 patentably define over the cited art as well.

Claims 3, 7, 10, 11 and 18 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schneider in view of Baldwin and further in view of Peercy, *et al.* (“Interactive Multi-Pass Programmable Shading” (ACM 2000), and “Peercy” hereinafter). It is respectfully submitted that claims 3, 7, 10, 11 and 18 are patentable for the reasons set forth below.

Peercy teaches interactive programmable shading using a scene graph library operating on top of OPENGL®. In operation, the OPENGL® architecture is treated as a general simple instruction multiple data (SIMD) computer and translate the high level shading description into OPENGL® rendering passes.

Applicant respectfully submits that Peercy fails to cure the deficiencies of Schneider and Baldwin, because at no point does Peercy appear to teach “*defining a temporary storage*

DOCKET NO.: MSFT-0992/191789.1
Application No.: 09/832,138
Office Action Dated: July 20, 2004

PATENT

requirement for a statically-allocated memory resource,” or “traversing [a] retained-mode representation according to [a] selected representational level and the defined temporary storage requirement to provide a final representation that can be rendered by a graphics pipeline” as claimed. Accordingly, Applicants respectfully submit that claims 3, 7, 10, 11 and 18 patentably define over the cited art.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that the pending claims patentably define over the prior art. Accordingly, a Notice of Allowance is respectfully requested. In the event that the Examiner believes that the present application is not allowable for any reason, the Examiner is encouraged to contact the undersigned attorney to discuss resolution of any remaining issues.

Date: October 20, 2004

Christos A. Ioannidi
Christos A. Ioannidi
Registration No. 54,195

Woodcock Washburn LLP
One Liberty Place - 46th Floor
Philadelphia PA 19103
Telephone: (215) 568-3100
Facsimile: (215) 568-3439